

Notice of Allowability

Application No.

10/687,247

Examiner

John H. Le

Applicant(s)

JONES ET AL.

Art Unit

2863



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
2. ☒ The allowed claim(s) is/are 1-21.
3. ☒ The drawings filed on 16 October 2003 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 03/31/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413),
Paper No./Mail Date 03/18/2005.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Anthony V.S. England on 03/18/2005.

The applicant has been amended as follows:

A value in a counter on a processor is incremented for occurrences of a monitored event, providing a measured value for the event. The value of the counter register for a first thread is saved responsive to a switch from the first thread to a second thread. The value is saved in an accumulator in system memory. Then, responsive to a switch back to the first thread, the value for the first thread is restored from the accumulator. In this way, a counter may be read, and its value, for the first thread, for example, ~~provides a coherent meaning relative to a previous value for the same thread,~~ remains consistent despite any intervening thread switches. Since the counter register may be read directly, in the user state, this provides a faster and more consistent means for updating way to update performance counts.

Reasons for Allowance

2. Claims 1-21 are allowed.

The following is an examiner's statement of reasons for allowance:

In combination with other limitations of the claims, the cited prior arts fails to teach steps of incrementing an N-bit value in one of the performance monitoring counter registers responsive to occurrences of a monitored event for a first processing thread so that the N-bit value provides a measured value for the event in association with the thread; merging the N-bit value of the counter register for the first processing thread into an N+M-bit value in an accumulator in system memory, wherein the merging is responsive to a switch from the first thread to a second thread; and restoring the N-bit value for the first thread to the counter register from the accumulator responsive to a switch back to the first thread, wherein despite any thread switches the restoring maintains a value in the counter register for the first thread that is coherent relative to a previous value in the counter register for the first thread and the merging of the N-bit value into the accumulator maintains a coherent value for the larger, N+M-bit accumulated value, as recited in claim(s) 1, 8, and 15.

U.S. Patent No. 6,016,466 discloses computer system for determining execution time for a portion of software includes obtaining a first time stamp value at a beginning of the portion, obtaining a second time stamp value at an end of the portion, adjusting at least one of the first and second time stamp values to compensate for any amount of time that the portion was swapped out in a multitasking operating system, and subtracting the first time stamp value from the second time stamp value to determine execution time. Determining execution time may also include providing a delta out value that is initialized to zero prior to the portion being run for a first time, incrementing the delta out value by an amount of time the portion is swapped out, compensating the

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first time stamp value by subtracting the delta out value therefrom, and compensating the second time stamp value by subtracting the delta out value therefrom. '466 fails to specify the steps of incrementing an N-bit value in one of the performance monitoring counter registers responsive to occurrences of a monitored event for a first processing thread so that the N-bit value provides a measured value for the event in association with the thread; merging the N-bit value of the counter register for the first processing thread into an N+M-bit value in an accumulator in system memory, wherein the merging is responsive to a switch from the first thread to a second thread; and restoring the N-bit value for the first thread to the counter register from the accumulator responsive to a switch back to the first thread, wherein despite any thread switches the restoring maintains a value in the counter register for the first thread that is coherent relative to a previous value in the counter register for the first thread and the merging of the N-bit value into the accumulator maintains a coherent value for the larger, N+M-bit accumulated value, as now recited in claims 1, 8, and 15 of the present invention.

US 2004/0123084 A1 discloses a method, system and program for tracing an instruction stream of a microprocessor, wherein the system comprising a processor includes a performance monitor with counter registers. The counter registers include a rep occurrence counter. According to a first option, the rep occurrence counter is set to count the occurrence of a repeat instruction by being programmed to one away from overflow. Upon detecting the occurrence of a repeat instruction, the counter increases and overflows, triggering an interrupt. According to a second option, the rep occurrence counter is set to count the occurrence of the last execution of a repeat instruction, which

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causes the counter to increase and overflow, triggering an interrupt. Another rep executions counter starts counting each execution of a repeat instruction upon detection of a repeat instruction. Thus, when the interrupt is triggered, the processor enables the trace program to read the rep executions counter, which has counted the actual number of times a repeat instruction executed. 'US 2004/0123084 A1 fails to specify the steps of incrementing an N-bit value in one of the performance monitoring counter registers responsive to occurrences of a monitored event for a first processing thread so that the N-bit value provides a measured value for the event in association with the thread; merging the N-bit value of the counter register for the first processing thread into an N+M-bit value in an accumulator in system memory, wherein the merging is responsive to a switch from the first thread to a second thread; and restoring the N-bit value for the first thread to the counter register from the accumulator responsive to a switch back to the first thread, wherein despite any thread switches the restoring maintains a value in the counter register for the first thread that is coherent relative to a previous value in the counter register for the first thread and the merging of the N-bit value into the accumulator maintains a coherent value for the larger, N+M-bit accumulated value, as now recited in claims 1, 8, and 15 of the present invention.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H. Le whose telephone number is 571-272-2275. The examiner can normally be reached on 7:00 - 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

March 18, 2005



John Barlow
Supervisory Patent Examiner
Technology Center 2800